Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1-10. (canceled)

11. (previously presented) A multilayer stack comprising:

a dielectric layer and one or more surrounding dielectric layers situated above or below the dielectric layer, a dielectric constant of the dielectric layer being greater than a dielectric constant of the surrounding dielectric layers, and

a metallization structure which is arranged on the dielectric layer and is arranged at a distance from a ground electrode, wherein the metallization structure has a capacitor electrode and a line that acts as a coil, where the capacitor electrode and the line are arranged in a common plane which lies parallel to the ground electrode at a distance h_1, and wherein:

$$\frac{w}{h_1} > 3,$$

where w is the width of the line, wherein:

$$\frac{\varepsilon_{medium} \cdot d_{\varepsilon}}{\varepsilon \cdot d_{medium}} > 5$$

wherein the dielectric constant of and a thickness of the dielectric layer are ε_{medium} and d_{medium}, respectively, and the dielectric constant of and a thickness of the surrounding dielectric layers are ε and d_{ε}, respectively.

12. (previously presented) A metallization structure as claimed in claim 11, further comprising:

a second ground electrode, the common plane comprising the capacitor electrode and the line being arranged parallel to said second ground electrode at a distance h_2, and the common plane comprising the capacitor electrode and the line being between the first and second ground electrodes, where

$$\frac{w}{h_2} > 3 .$$

13. (previously presented) A multilayer stack as claimed in claim 12, further comprising one or more additional metallization structures in the common plane, wherein

$$\frac{\varepsilon_{medium} \cdot d_{\min}}{\varepsilon \cdot d_{medium}} > 7 ,$$

where d_{min} is the minimum distance to a nearest metallization structure in the plane, and wherein the dielectric constant of and a thickness of the dielectric layer are ε_{medium} and d_{medium}, respectively, and the dielectric constant of the surrounding dielectric layers is ε.

14. (previously presented) A multilayer stack as claimed in claim 12, wherein the multilayer stack comprises magnetic layers.

15. (previously presented) A multilayer stack as claimed in claim 12, produced in a multilayer laminate process.

16. (previously presented) A multilayer stack as claimed in claim 12, produced in a Low Temperature Cofire Ceramic (LTCC) process.

17. (previously presented) A multilayer stack comprising:

a dielectric layer and one or more surrounding dielectric layers situated above or below the dielectric layer, a dielectric constant of the dielectric layer being greater than a dielectric constant of the surrounding dielectric layers, and

a metallization structure which is arranged on the dielectric layer and is arranged at a distance from a ground electrode, wherein the metallization structure has a capacitor electrode and a line that acts as a coil, where the capacitor electrode and the line are arranged in a common plane which lies parallel to the ground electrode at a distance h_1, and wherein:

$$\frac{w}{h_1} > 3,$$

where w is the width of the line, wherein the multilayer stack is produced in a Low Temperature Cofire Ceramic (LTCC) process.

18. (previously presented) A metallization structure as claimed in claim 17, further comprising:

a second ground electrode, the common plane comprising the capacitor electrode and the line being arranged parallel to said second ground electrode at a distance h_2, and the common plane comprising the capacitor electrode and the line being between the first and second ground electrodes, where

$$\frac{w}{h_2} > 3.$$

19. (previously presented) A multilayer stack as claimed in claim 18, further comprising one or more additional metallization structures in the common plane, wherein

$$\frac{\varepsilon_{medium} \cdot d_{\min}}{\varepsilon \cdot d_{medium}} > 7,$$

where d_{min} is the minimum distance to a nearest metallization structure in the plane, and wherein the dielectric constant of and a thickness of the dielectric layer are ε_{medium} and d_{medium}, respectively, and the dielectric constant of the surrounding dielectric layers is ε.

20. (previously presented) A multilayer stack as claimed in claim 18, wherein the multilayer stack comprises magnetic layers.

21. (previously presented) A multilayer stack as claimed in claim 18, produced in a multilayer laminate process.

22. (new) A multilayer stack comprising:

a dielectric layer and one or more surrounding dielectric layers situated above or below the dielectric layer, a dielectric constant of the dielectric layer being greater than a dielectric constant of the surrounding dielectric layers;

a second ground electrode, the common plane comprising the capacitor electrode and the line being arranged parallel to said second ground electrode at a distance h_2, and the common plane comprising the capacitor electrode and the line being between the first and second ground electrodes, where

$$\frac{w}{h_2} > 3;$$

a metallization structure which is arranged on the dielectric layer and is arranged at a distance from a ground electrode, wherein the metallization structure has a capacitor electrode and a line that acts as a coil, where the capacitor electrode and the line are arranged in a common plane which lies parallel to the ground electrode at a distance h_1, and wherein

$$\frac{w}{h_1} > 3,$$

where w is the width of the line; and

one or more additional metallization structures in the common plane, wherein

$$\frac{\varepsilon_{medium} \cdot d_{\min}}{\varepsilon \cdot d_{medium}} > 7,$$

where d_{min} is the minimum distance to a nearest metallization structure in the plane, and wherein the dielectric constant of and a thickness of the dielectric layer are ε_{medium} and d_{medium}, respectively, and the dielectric constant of the surrounding dielectric layers is ε.

23. (new) The multilayer stack of claim 22,

$$\frac{\varepsilon_{medium} \cdot d_{\varepsilon}}{\varepsilon \cdot d_{medium}} > 5$$

wherein the dielectric constant of and a thickness of the dielectric layer are ε_{medium} and d_{medium}, respectively, and the dielectric constant of and a thickness of the surrounding dielectric layers are ε and d_{ε}, respectively.

24. (new) The multilayer stack of claim 22, wherein the multilayer stack comprises magnetic layers.

25. (new) The multilayer stack of claim 22, wherein the multilayer stack is produced in a multilayer laminate process.

26. (new) The multilayer stack of claim 22, wherein the multilayer stack is produced in a LTCC process.

27. (new) A multilayer stack comprising:

magnetic layers;

a dielectric layer and one or more surrounding dielectric layers situated above or below the dielectric layer, a dielectric constant of the dielectric layer being greater than a dielectric constant of the surrounding dielectric layers;

a second ground electrode, the common plane comprising the capacitor electrode and the line being arranged parallel to said second ground electrode at a distance h_2, and the common plane comprising the capacitor electrode and the line being between the first and second ground electrodes, where

$$\frac{w}{h_2} > 3 \text{; and}$$

a metallization structure which is arranged on the dielectric layer and is arranged at a distance from a ground electrode, wherein the metallization structure has a capacitor electrode and a line that acts as a coil, where the capacitor electrode and the line are

arranged in a common plane which lies parallel to the ground electrode at a distance h_1, and wherein

$$\frac{w}{h_1} > 3,$$

where w is the width of the line.

28. (new) The multilayer stack of claim 27,

$$\frac{\varepsilon_{medium} \cdot d_{\varepsilon}}{\varepsilon \cdot d_{medium}} > 5$$

wherein the dielectric constant of and a thickness of the dielectric layer are ε_{medium} and d_{medium}, respectively, and the dielectric constant of and a thickness of the surrounding dielectric layers are ε and d_{ε}, respectively.

29. (new) The multilayer stack of claim 27, wherein the multilayer stack is produced in a multilayer laminate process.

30. (new) The multilayer stack of claim 27, wherein the multilayer stack is produced in a LTCC process.